a pixel switch for selectively providing the image signals to a third electrode from a first electrode connected to the source signal line depending on voltage state of a second electrode connected to the scan signal line;

a power unit for respectively supplying first power and second power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit including a first control signal line for transmitting a first control signal to all pixels from outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from the outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting according to voltage difference between the image signals and the second power; and

a memory cell unit for receiving the first control signal and the second control signal from the control signal line unit.

2. (Amended) The liquid crystal display (LCD) of claim 1, wherein an operation mode image signal output by the third electrode of the pixel switch is transmitted to the liquid crystal unit, when the first control signal is in low state and the second control signal is in high state, and when the first control signal is in high state.

3. (Amended) The liquid crystal display (LCD) of claim 1, wherein the memory cell unit further comprises:

a first inverter circuit including a nTFT and a pTFT, a drain electrode of the nTFT is connected to the pTFT, and gate electrodes of the first inverter circuit are connected to the third electrode of the pixel switch;

a second inverter circuit including a nTFT and a pTFT, drain electrodes of the second inverter circuit are connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit are connected to the drain electrodes of the first inverter circuit;

a push nTFT including a drain electrode connected to the first power, a source electrode connected to a source electrode of the pTFTs of the first and second inverter circuits and a gate electrode of the push nTFT connected to the first control signal line;

a pull nTFT including a source electrode connected to the second power, a drain electrode connected to source electrodes of the nTFTs of the first and second inverter circuit and a gate electrode of the pull nTFT connected to the first control signal line;

an operation nTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT are connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still pTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the still pTFT connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

4. (Amended) The liquid crystal display (LCD) of claim 1, wherein the control signal line unit transmits control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions.

5. (Amended) A low power liquid crystal display (LCD), comprising:

a scan signal line for supplying scanning signals to pixels configuring an LCD panel;

a source signal line for supplying image signals to pixels configuring the LCD panel;

a pixel switch for selectively outputting the image signals to a third electrode from a first electrode connected to the source signal line depending on voltage state of a second electrode connected to the scan signal line;

a power unit for supplying a first power, a second power and a third power to all pixels from outside of a pixel area of the LCD panel;

a control signal line unit including a first control signal line for transmitting a first control signal to all pixels from the outside of the pixel area of the LCD panel, and a second control signal line for transmitting a second control signal to all pixels from outside of the pixel area of the LCD panel;

a liquid crystal unit for selectively transmitting according to a difference between the image signals and the third power; and

a level shift unit for receiving the second control signal, lifting the high state by as much as the second power, generating an inverting signal, and outputting the inverting signal.

6. (Amended) The liquid crystal display (LCD) of claim 5, further comprising a memory cell unit.

7. (Amended) The liquid crystal display (LCD) of claim 6, wherein the memory cell unit receives the first and second control signals from the control signal line unit and receiving the inverting signal of the second control signal output by the level shift unit.

8. (Amended) The liquid crystal display of (LCD) claim 7, wherein an operation mode image signal is selectively output by a third electrode of the pixel switch and the operation mode signal is selectively transmitted to the liquid crystal unit.

A1

9. (Amended) The liquid crystal display (LCD) of claim 7, wherein the memory cell unit comprises:

a first inverter circuit including a nTFT and a pTFT, a drain electrode of the nTFT connected to the pTFT, and gate electrodes of the first inverter circuit are connected to the third electrode of the pixel switch;

a second inverter circuit including a nTFT and a pTFT, drain electrodes of the nTFT and pTFT connected to the third electrode of the pixel switch, and gate electrodes of the second inverter circuit nTFT and pTFT are connected to the drain electrodes of the first inverter circuit;

a push nTFT including a drain electrode connected to the first power, a source electrode connected to source electrodes of the pTFTs of the first and second inverter circuits, and a gate electrode connected to the first control signal line;

a pull nTFT including a source electrode connected to the third power, a drain electrode connected to source electrodes of the nTFTs of the first and second inverter circuits and the second inverter circuit, and a gate electrode connected to the first control signal line;

an operation nTFT including a gate electrode connected to the second control signal line, and source and drain electrodes of the operation nTFT connected between the third electrode of the pixel switch and the liquid crystal unit; and

a still nTFT having a gate electrode connected to receive an inverting signal of the second control signal output by the level shift unit, and source and drain electrodes of the still nTFT connected between the drain electrode of the first inverter circuit and the liquid crystal unit.

10. (Amended) The liquid crystal display (LCD) of claim 5, wherein the level shift unit comprises:

a third inverter circuit having an nTFT and a pTFT, a drain electrode of the nTFT is connected to that of the pTFT of the third inverter circuit, gate electrodes are connected to the second control signal line, a source electrode of the pTFT is connected to the second power, and a source electrode of the nTFT is connected to the third power; and

a level-up pTFT having a gate electrode connected to a drain electrode of the third inverter circuit, a source electrode of the level-up pTFT is connected to the second power, and a drain electrode of the level-up pTFT is connected to the second control signal line.

11. (Amended) The liquid crystal display (LCD) of claim 5, wherein the control signal line unit transmits respective control signals sequentially delayed by a buffer circuit to corresponding pixel areas when the pixel area of the LCD panel is divided into at least two portions.

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12. (Not Amended) In a liquid crystal display (LCD) panel driving method for a pixel switch that receives scanning signals and image signals from scanning signal lines and source signal lines to output the image signals to a memory cell unit that is operated by first and second

control signals or stops the image signals to display the same, an LCD driving method comprising:

the memory cell unit transmitting operation mode image signals output by the pixel switch to liquid crystal and displaying the same when the first control signal is in low state and the second control signal is in high state; and

transmitting either a still mode image signal output by a third electrode of the pixel switch or its inverting signal to the liquid crystal as the second control signal periodically repeats low and high states to fit characteristics of an LCD panel when the first control signal is in high state.

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13. (Amended) The method of claim 12, wherein the method further comprises transmitting respective control signals sequentially delayed by a buffer circuit to a corresponding pixel area when the pixel area of the LCD panel is divided into at least two portions in either a horizontal or vertical direction.

A2

Please **ADD** the following new claims:

--14. (New) The liquid crystal display of (LCD) claim 7, wherein a still mode image signal is selectively output by the third electrode of the pixel switch.

A3

15. (New) The liquid crystal display of (LCD) claim 7, wherein an inverting signal is selectively transmitted to the liquid crystal unit as the second control signal periodically repeats the low and high states according to characteristics of the LCD panel.

16. (New) A liquid crystal display (LCD), comprising:

a scan signal line;

a source signal line;

a pixel switch for selectively outputting image signals;

a power unit for supplying a first power, a second power and a third power to pixels;

a first control signal line for transmitting a first control signal to the pixels;

a second control signal line for transmitting a second control signal to the pixels; and

a level shift unit in electrical communication with the second control signal for generating an inverting signal.

17. (New) A liquid crystal display (LCD) of claim 16, wherein the level shift unit outputs the generated inverting signal.

18. (New) A liquid crystal display, comprising:

a scan driver activated to supply scanning signals for a first period and inactivated for a second period;

a source driver activated to supply image signals for the first period and inactivated for the second period; and

a plurality of pixels, each pixel including a liquid crystal capacitor displaying an image, a pixel switch for transmitting the image signals in response to the scanning signal, and a memory cell storing and transmitting the image signal from the pixel switch to the liquid crystal capacitor during the first period and providing at least one of the stored image signal and an inversion signal to the stored image signal for the liquid crystal capacitor during the second period. –